What is claimed is:

1. A method of processing a plurality of Z vectors, each Z vector including Z elements, each element including K bits, where Z is a positive integer greater than 1 and K is a positive integer greater than zero, the plurality of Z vectors corresponding to a binary codeword, portions of said binary codeword having a direct mapping relationship to a plurality of transmission units, said plurality of Z vectors being stored in a set of D memory arrays, where D is an integer greater than zero, each memory array including Z rows of memory locations, each memory location of a row corresponding to a different array column, each array column corresponding to a different one of said plurality of Z vectors, each Z vector identifying one column in each of said D memory arrays, the method comprising:

generating a series of sets of control information, each set of control information including:

i) a transmission unit identifier;

ii) a Z vector identifier;

iii) a row identifier; and

for at least one generated set of control information:

reading P times K divided by D bits, where P is a positive integer greater than zero, from each column identified by the Z vector identified by the Z vector identifier included in said at least one generated set of control information.

2. The method of claim 1,

wherein said method of processing is performed by a transmission device prior to transmission of said transmission units;

wherein D is 1; and

wherein K is 1.

3. The method of claim 2, further comprising:

for said at least one generated set of control information:

generating from said P bits read from memory, a portion of the transmission unit identified by the transmission unit identifier included in said at least one generated set of control information.

4. The method of claim 3,

wherein said plurality of Z vectors includes n of said plurality of Z vectors, where n is a positive integer greater than 1; and

wherein generating a series of sets of control information further includes:

incrementing a Z vector identifier value by n divided by M, where M is the number of portions of the transmission unit having a direct mapping relationship to a portion of the binary codeword said portion of the binary codeword including M times P bits.

5. The method of claim 4,

wherein each portion of a transmission unit is a symbol; and

wherein the transmission unit is a dwell.

6. The method of claim 3, wherein generating a series of sets of control information further includes:

incrementing the Z vector identifier value M times;

after incrementing the Z vector value M times:

i) resetting the Z vector identifier value to the Z vector identifier value existing at the start of said incrementing; and

ii) incrementing a row identifier value by P.

7. The method of claim 6, wherein generating a series of sets of control information further includes:

after incrementing the row identifier value Z divided by P times, where Z divided by P times is an integer,

setting the row identifier value to zero; and

incrementing the Z vector identifier value by a preselected positive integer value.

8. The method of claim 7, wherein said preselected positive integer value is one.

9. The method of claim 2, wherein said binary codeword is a low density parity check codeword.

10. The method of claim 1,

wherein said method of processing is used to process received transmission units; and

wherein K is an integer greater than zero and is a number of bits used to represent a soft value corresponding to one bit of said binary codeword.

11. The method of claim 10, where D is equal to K or 1.

12. The method of claim 11, further comprising:

for said at least one generated set of control information:

supplying the P bits read from memory to a demodulator.

13. The method of claim 10, further comprising:

for said at least one generated set of control information:

generating from said P bits read from memory, a portion of the transmission unit identified by the transmission unit identifier included in said each generated set of control information.

14. The method of claim 13,

wherein said plurality of Z vectors includes n of said Z vectors, where n is a positive integer greater than 1; and

wherein generating a series of sets of control information further includes:

incrementing a Z vector identifier value n divided by M, where M is the number of portions of the transmission unit having a mapping relationship to a portion of the binary codeword said portion of the binary codeword including M times P bits.

15. The method of claim 13, wherein generating a series of sets of control information further includes:

incrementing a row identifier value by P incrementing the Z vector identifier value M times;

after incrementing the Z vector value M times:

i) resetting the Z vector identifier value to the Z vector identifier value existing at the start of said incrementing; and

ii) incrementing a row identifier value by P.

16. The method of claim 15, wherein generating a series of sets of control information further includes:

after incrementing the row identifier value Z divided by P times, where Z divided by P times is an integer,

setting the row identifier value to zero; and

incrementing the Z vector identifier value by a preselected positive integer value.

17. The method of claim 16, wherein said preselected positive integer value is one.

18. The method of claim 10, wherein said binary codeword is a low density parity check codeword.

19. An apparatus for processing a plurality of Z vectors, each Z vector including Z elements, each element including K bits, where Z is a positive integer greater than 1 and K is a positive integer greater than zero, the plurality of Z vectors corresponding to a binary codeword, portions of said binary codeword having a direct mapping relationship to a plurality of transmission units, said apparatus comprising:

memory including a set of D memory arrays for storing said plurality of Z vectors, where D is an integer greater than zero, each memory array including Z rows of memory locations, each memory location of a row corresponding to a different array column, each array column corresponding to a different one of said plurality of Z vectors, each Z vector identifying one column in each of said D memory arrays;

memory access control module for generating a series of sets of control information, each set of control information including:

i) a transmission unit identifier;

ii) a Z vector identifier;

iii) a row identifier; and

means for reading P times K divided by D bits, from said memory, where P is a positive integer greater than zero, from each column identified by the Z vector identified by the Z vector identifier included at least one generated set of control information.

20. The method of claim 1,
wherein D is 1; and
wherein K is 1.

21. The method of claim 19, wherein said memory access control modules includes:
a first counter for generating said Z vector identifier; and
a second counter for generating said row identifier.

22. A machine readable medium comprising machine executable instructions for controlling a computer device to process a plurality of Z vectors, each Z vector including Z elements, each element including K bits, where Z is a positive integer greater than 1 and K is a positive integer greater than zero, the plurality of Z vectors corresponding to a binary codeword, portions of said binary codeword having a direct mapping relationship to a plurality of transmission units, said machine executable instructions including instructions used to control the computer device to:
generate a series of sets of control information, each set of control information including:
i) a transmission unit identifier;
ii) a Z vector identifier; and
iii) a row identifier; and
for at least one generated set of control information:
read P times K divided by D bits, where P is a positive integer greater than zero, from each column identified by the Z vector identified by the Z vector identifier included in said at least one generated set of control information.